Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL/MAY 2026

Fifth Semester

Electronics and Communication Engineering

EC3552- VLSI AND CHIP DESIGN

Regulations - 2021

Duration: 3 Hrs. *Maximum: 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	How does a MOSFET act as a switch?	L1	1	2
2.	Identify the need for scaling in the CMOS inverter.	L1	1	2
3.	Draw the stick diagram for a two-input NAND gate.	L1	2	2
4.	List the disadvantages of pass transistor logic.	L1	2	2
5.	Define Pipelining.	L1	3	2
6.	Identify the timing classification of a digital system.	L1	3	2
7.	Give the applications of high-speed adders.	L1	4	2
8.	Compare ROM and PLA.	L2	4	2
9.	List the basic steps in the wafer chip fabrication process flow.	L1	5	2
10.	Write the test bench in Verilog HDL to test the D-flip-flop.	L2	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Develop the ideal I-V characteristics and non-ideal I-V characteristics of an NMOS and PMOS device.	L3	1	16
			Or			
	b		Identify the dynamic behavior of the MOSFET transistor with a neat diagram.	L3	1	16
12.	a	i	Explain Elmore's constant for a 4-input NAND gate.	L2	2	8
		ii	Summarize the features of static CMOS logic.	L2	2	8
			Or			
	b	i	Discuss the disadvantages of dynamic logic gates and list the solutions to overcome the disadvantages.	L2	2	8
		ii	Illustrate the low-power design principles of CMOS circuits.	L2	2	8
13.	a		Explain the methodology of sequential circuits of latches and registers.	L2	3	16
			Or			
	b		Explain a monostable sequential circuit with a neat circuit diagram.	L2	3	16

14.	a		Design a 16-bit carry-bypass and carry-select adder, and discuss its features.	L3	4	16
			Or			
	b		Identify the hierarchical memory architecture and describe its building blocks.	L3	4	16
15.	a	i	Illustrate the ASIC Design flow with a neat diagram.	L2	5	8
		ii	Outline the microchip design process and identify the issue in the test.	L2	5	8
			Or			
	b		Explain the three main approaches commonly used for design for testability.	L2	5	16